

ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

Title of Invention

Integrated Circuit Chip Having A Ringed Wiring Layer Interposed
Between A Contact Layer And A Wiring Grid

Application Number :

Confirmation Number:

First Named Applicant: Thomas Bednar

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Art Unit:

Examiner:

Search string: (6202191 or 6185722 or 6184477 or 6182272 or 6035111 or 6028440 or 6002857
or 5978572 or 5923089 or 5793643 or 5404310 or 5283753 or 5272645 or 5145800
or 5040144).pn

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
	1	6202191	2001-03-27	Filippi et al			
	2	6185722	2001-02-06	Darden et al			
	3	6184477	2001-02-06	Tanahashi			
	4	6182272	2001-01-30	Andreev et al			
	5	6035111	2000-03-07	Suzuki et al			
	6	6028440	2000-02-22	Roethig et al			
	7	6002857	1999-12-14	Ramachandran			
	8	5978572	1999-11-02	Toyonaga et al			
	9	5923089	1999-07-13	Yao et al			
	10	5793643	1998-08-11	Cai			
	11	5404310	1995-04-04	Mitsubishi			
	12	5283753	1994-02-01	Schucker et al			
	13	5272645	1993-12-21	Kawakami et al			
	14	5145800	1992-09-08	Arai et al			
	15	5040144	1991-08-13	Pelley et al			

Signature

Examiner Name

Date